CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Zilog SCC Serial Communication Controller is a dual channel, multiprotocol data communication peripheral designed for use with 8- and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The SCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem control in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (the number of the registers varies depending on the version), the user can configure the SCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements.

Within each operating mode, the SCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The SCC/ESCC family consists of the following seven devices;

	Z-Bus®	Universal-Bus
NMOS	Z8030	Z8530
CMOS	Z80C30	Z85C30
ESCC	Z80230	Z85230
EMSCC		Z85233

As a convention, use the following words to distinguish the devices throughout this document.

SCC: Description applies to all versions.

NMOS: Description applies to NMOS version (Z8030/Z8530)

CMOS: Description applies to CMOS version (Z80C30/Z85C30)

ESCC: Description applies to ESCC (Z80230/Z85230)

EMSCC: Description applies to EMSCC (Z85233)

Z80X30: Description applies to Z-Bus version of the device (Z8030/Z80C30/Z80230)

Z85X3X: Description applies to Universal version of the device (Z8530/Z85C30/Z85230/Z85233)

The Z-Bus version has a multiplexed bus interface and is directly compatible with the Z8000, Z16C00 and 80x86 CPUs. The Universal version has a non-multiplexed bus interface and easily interfaces with virtually any CPU, including the 8080, Z80, 68X00.

1.2 SCC'S CAPABILITIES

The NMOS version of the SCC is Zilog's original device. The design is based on the Z80 SIO architecture. If you are familiar with the Z80 SIO, the SCC can be treated as an SIO with support circuitry such as DPLL, BRG, etc. Its features include:

- Two independent full-duplex channels
- Synchronous/Isosynchronous data rates:
  - Up to 1/4 of the PCLK using external clock source.
    Up to 5 Mbits/sec at 20 MHz PCLK (ESCC)
    Up to 4 Mbits/sec at 16 MHz PCLK (CMOS)
    Up to 2 MBits/sec at 8 MHz PCLK (NMOS)
  - Up to 1/8 of the PCLK (up to 1/16 on NMOS) using FM encoding with DPLL
  - Up to 1/16 of the PCLK (up to 1/32 on NMOS) using NRZI encoding with DPLL
- Asynchronous Capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less.)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit
- Receiver FIFO
  ESCC: 8 bytes deep
  NMOS/CMOS: 3 bytes deep
- Transmitter FIFO
  ESCC: 4 bytes deep
  NMOS/CMOS: 1 byte deep
- NRZ, NRZI or FM encoding/decoding. Manchester code decoding (encoding with external logic).
- Baud Rate Generator in each channel
- Digital Phase Locked Loop (DPLL) for clock recovery
- Crystal oscillator

The CMOS version of the SCC is 100% plug in compatible to the NMOS versions of the device, while providing the following additional features:

- Status FIFO
- Software interrupt acknowledge feature
- Enhanced timing specifications
- Faster system clock speed
- Designed in Zilog's Superintegration™ core format
- When the DPLL clock source is external, it can be up to 2x the PCLK, where NMOS allows up to PCLK (32.3 MHz max with 16/20 MHz version).

The Z85C30 CMOS SCC has added new features, while maintaining 100% hardware/software compatibility. It has the following new features:

- New programmable WR7' (write register 7 prime) to enable new features.
- Improvements to support SDLC mode of synchronous communication:
  - Improved functionality to ease sending back-to back frames
  - Automatic SDLC opening Flag transmission*
  - Automatic Tx Underrun/EOM Latch reset in SDLC mode*
  - Automatic /RTS deactivation*
  - TxD pin forced "H" in SDLC NRZI mode after closing flag*
  - Complete CRC reception*
  - Improved response to Abort sequence in status FIFO
  - Automatic Tx CRC generator preset/reset
  - Extended read for write registers*
  - Write data setup timing improvement
- Improved AC timing:
  - Three to 3.5 PCLK access recovery time.
  - Programmable /DTR//REQ timing*
  - Elimination of write data to falling edge of /WR setup time requirement
  - Reduced /INT timing
- Other features include:
  - Extended read function to read back the written value to the write registers*
  - Latching RR0 during read
  - RR0, bit D7 and RR10, bit D6 now has reset defaultvalue.

Some of the features listed above are available by default, and some of them (features with "*") are disabled on default.

ESCC (Enhanced SCC) is pin and software compatible to the CMOS version, with the following additional enhancements.

- Deeper transmit FIFO (4 bytes)
- Deeper receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced high with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

1.3 BLOCK DIAGRAM

Figure 1-1 has the block diagram of the SCC. Note that the depth of the FIFO differs depending on the version. The 10X19 SDLC Frame Status FIFO is not available on the NMOS version of the SCC.

Detailed internal signal path will be discussed in Chapter 4.

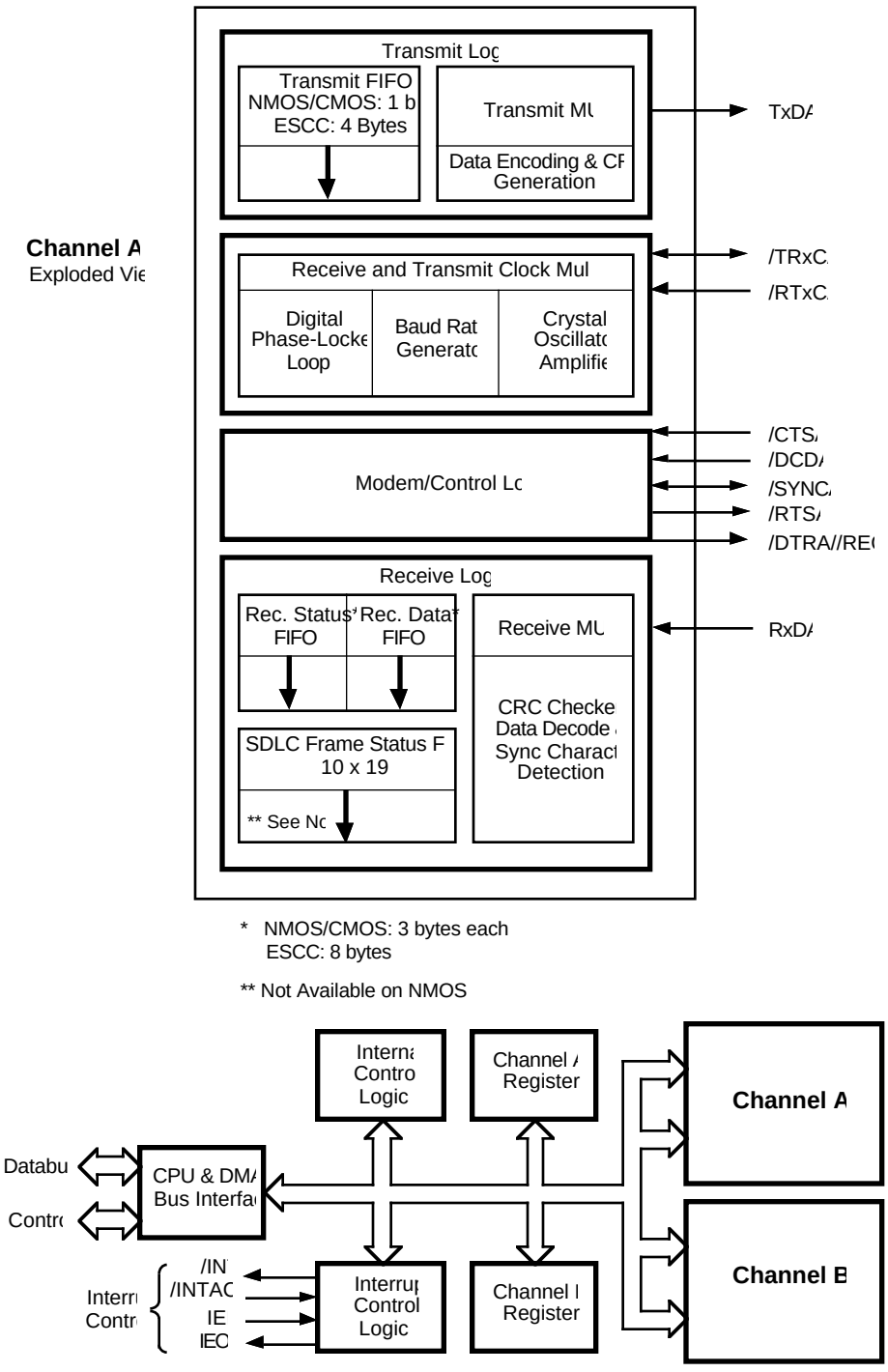

Figure 1-1. SCC Block Diagram

1.4 PIN DESCRIPTIONS

The SCC pins are divided into seven functional groups: Address/Data, Bus Timing and Reset, Device Control, Interrupt, Serial Data (both channels), Peripheral Control (both channels), and Clocks (both channels). Figures 1-2 and 1-3 show the pins in each functional group for both Z80X30 and Z85X30. Notice the pin functions unique to each bus interface version in the Address/Data group, Bus Timing and Reset group, and Control groups.

The Address/Data group consists of the bidirectional lines used to transfer data between the CPU and the SCC (Addresses in the Z80X30 are latched by /AS). The direction of these lines depends on whether the operation is a Read or Write.

The timing and control groups designate the type of transaction to occur and when it will occur. The interrupt group provides inputs and outputs to conform to the Z-Bus® specifications for handling and prioritizing interrupts. The remaining groups are divided into channel A and channel B groups for serial data (transmit or receive), peripheral control (such as DMA or modem), and the input and output lines for the receive and transmit clocks.

The signal functionality and pin assignments (Figures 1-4 to 1-7) stay constant within the same bus interface group (i.e., Z80X30, Z85X30), except for some timing and/or DC specification differences. For details, please reference the individual product specifications.

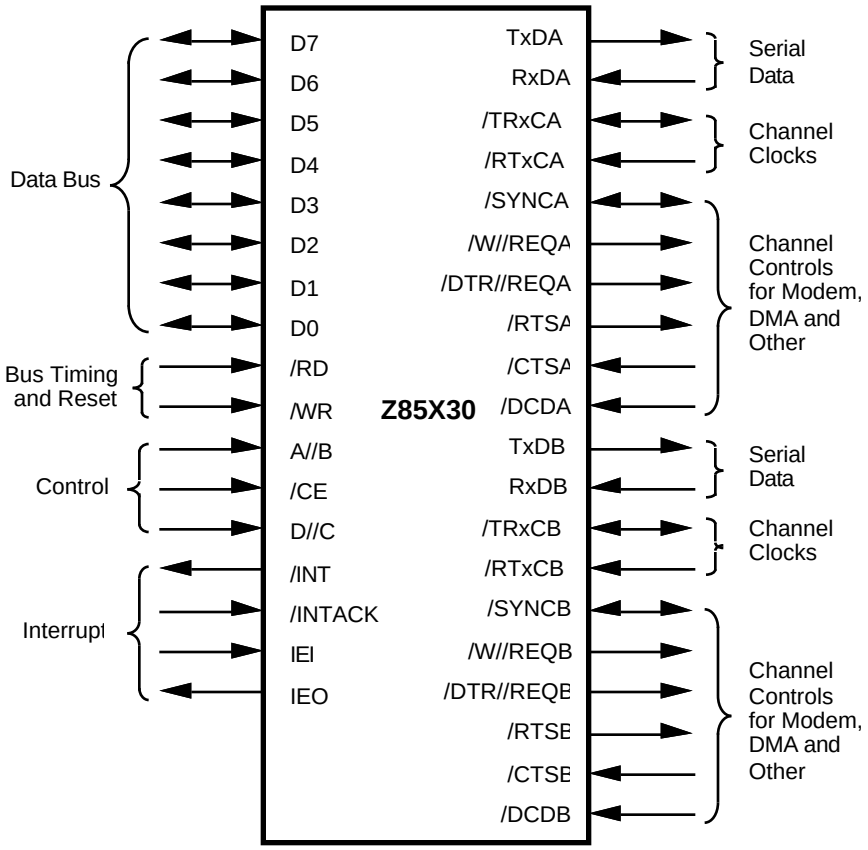

Figure 1-2. Z85X30 Pin Functions

1.4 PIN DESCRIPTIONS (Continued)

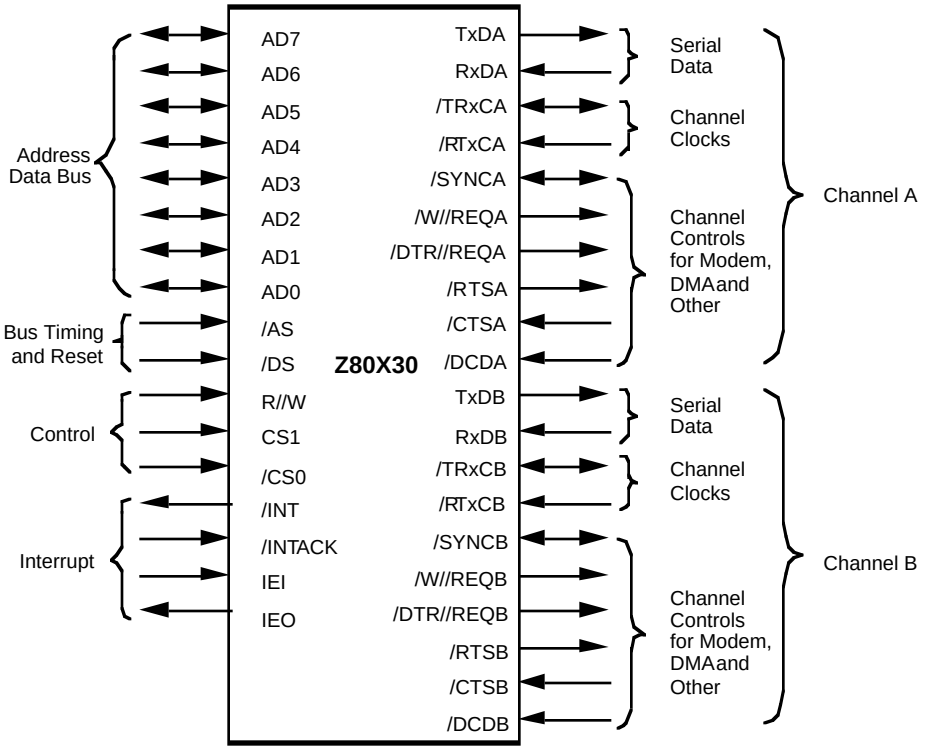

Figure 1-3. Z80X30 Pin Functions

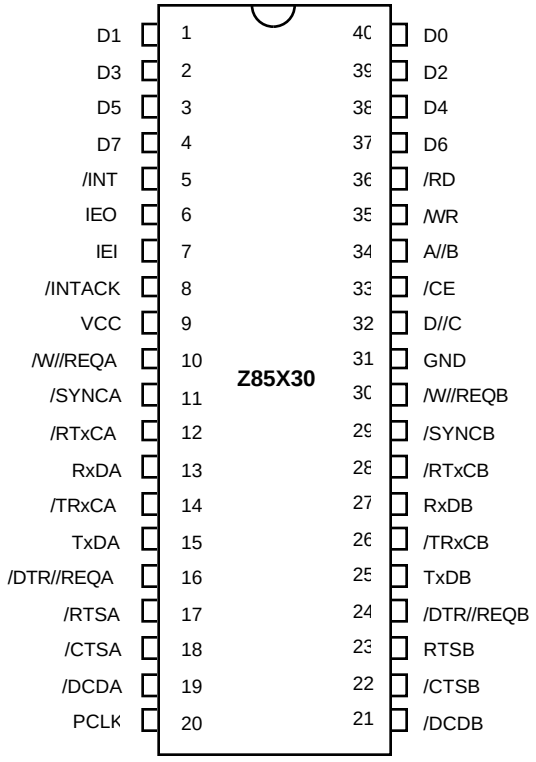

Figure 1-4. Z85X30 DIP Pin Assignments

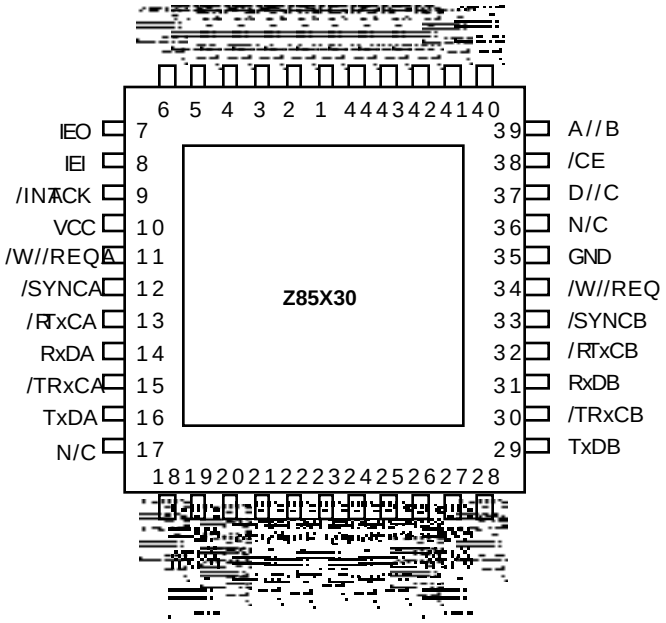

Figure 1-5. Z85X30 PLCC Pin Assignments

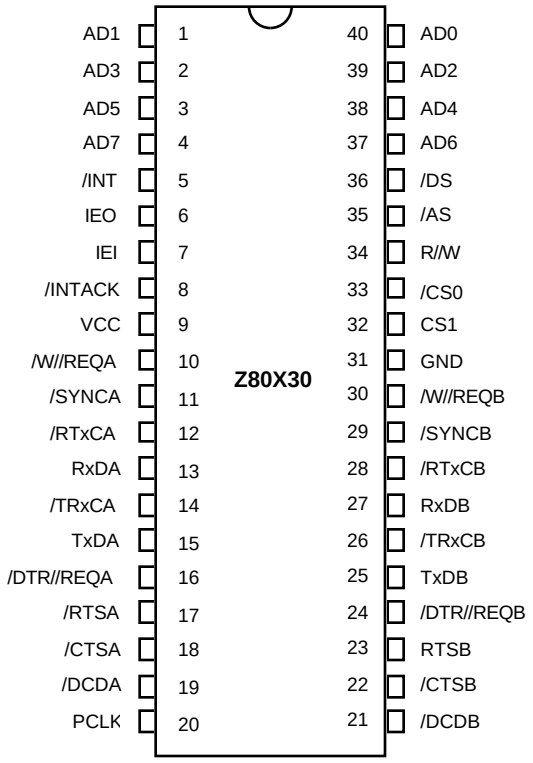

Figure 1-6. Z80X30 DIP Pin Assignments

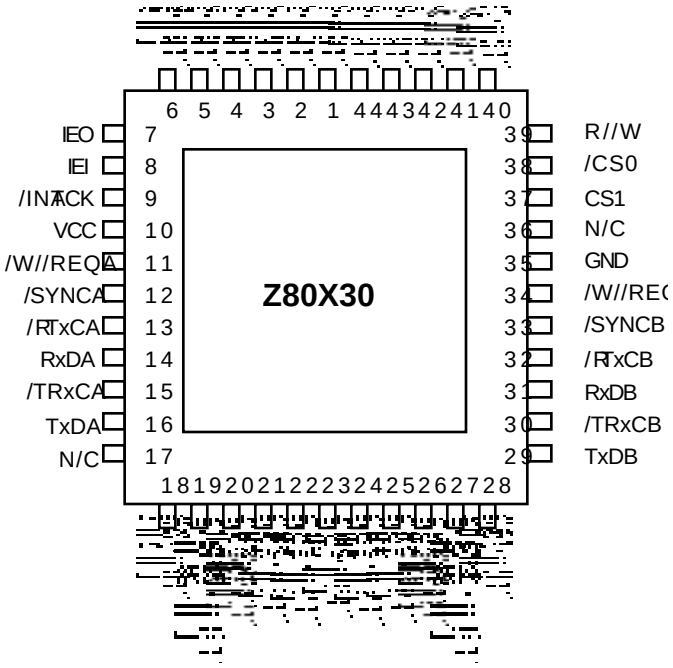

Figure 1-7. Z80X30 PLCC Pin Assignments

1.4.1 Pins Common to both Z85X30 and Z80X30

/CTSA, /CTSB. Clear To Send (inputs, active Low). These pins function as transmitter enables if they are programmed for Auto Enable (WR3, D5=1). A Low on the inputs enables the respective transmitters. If not programmed as Auto Enable, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC detects pulses on these inputs and can interrupt the CPU on both logic level transitions.

/DCDA, /DCDB. Data Carrier Detect (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enable (WR3, D5=1); otherwise, they are used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise time signals. The SCC detects pulses on these pins and can interrupt the CPU on both logic level transitions.

/RTSA, /RTSB. Request To Send (outputs, active Low). The /RTS pins can be used as general-purpose outputs or with the Auto Enable feature. When used with Auto Enable ON (WR3, D5=1) in asynchronous mode, the /RTS pin goes High after the transmitter is empty. When Auto Enable is OFF, the /RTS pins are used as general-purpose outputs, and, they strictly follow the inverse state of WR5, bit D1.

ESCC and 85C30:
In SDLC mode, the /RTS pins can be programmed to be deasserted when the closing flag of the message clears the TxD pin, if WR7' D2 is set.

/SYNCA, /SYNCB. Synchronization (inputs or outputs, active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to CTS and DCD. In this mode, transitions on these lines affect the state of the Synchronous/Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode, with the crystal oscillator not selected, these lines also act as inputs. In this mode, /SYNC is driven Low to receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of SYNC.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the

1.4 PIN DESCRIPTIONS (Continued)

receive clock cycle in which the synchronous condition is not latched. These outputs are active each time a synchronization pattern is recognized (regardless of character boundaries). In SDLC mode, the pins act as outputs and are valid on receipt of a flag. The /SYNC pins switch from input to output when monosync, bisync, or SDLC is programmed in WR4 and sync modes are enabled.

/DTR//REQA, /DTR//REQB. Data Terminal Ready/Request (outputs, active Low). These pins are programmable (WR14, D2) to serve either as general-purpose outputs or as DMA Request lines. When programmed for DTR function (WR14 D2=0), these outputs follow the state programmed into the DTR bit of Write Register 5 (WR5 D7). When programmed for Ready mode, these pins serve as DMA Requests for the transmitter.

ESCC and 85C30:
When used as DMA request lines (WR14, D2=1), the timing for the deactivation request can be programmed in the added register, Write Register 7' (WR7') bit D4. If this bit is set, the /DTR//REQ pin is deactivated with the same timing as the /W/REQ pin. If WR7' D4 is reset, the deactivation timing of /DTR//REQ pin is four clock cycles, the same as in the Z85C30.

/W//REQA, /W//REQB. Wait/Request (outputs, open-drain when programmed for Wait function, driven High or Low when programmed for Ready function). These dual-purpose outputs may be programmed as Request lines for a DMA controller or as Wait lines to synchronize the CPU to the SCC data rate. The reset state is Wait.

RxDA, RxDB. Receive Data (inputs, active High). These input signals receive serial data at standard TTL levels.

/RTxCA, /RTxCB. Receive/Transmit Clocks (inputs, active Low). These pins can be programmed to several modes of operation. In each channel, /RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

TxDA, TxDB. Transmit Data (outputs, active High). These output signals transmit serial data at standard TTL levels.

/TRxCA, /TRxCB. Transmit/Receive Clocks (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. /TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the Transmit Clock Counter (which parallels the Digital Phase-Locked Loop), the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

PCLK. Clock (input). This is the master SCC clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.

IEI. Interrupt Enable In (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. Interrupt Enable Out (output, active High). IEO is High only if IEI is High and the CPU is not servicing the SCC interrupt or the SCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

/INT. Interrupt (output, open drain, active Low). This signal is activated when the SCC requests an interrupt. Note that /INT is an open-drain output.

/INTACK. Interrupt Acknowledge (input, active Low). This is a strobe which indicates that an interrupt acknowledge cycle is in progress. During this cycle, the SCC interrupt daisy chain is resolved. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending. During the acknowledge cycle, if IEI is high, the SCC places the interrupt vector on the databus when /RD goes active. /INTACK is latched by the rising edge of PCLK.

1.4.2 Pin Descriptions, (Z85X30 Only)

D7-D0. Data bus (bidirectional, tri-state). These lines carry data and commands to and from the Z85X30.

/CE. Chip Enable (input, active Low). This signal selects the Z85X30 for a read or write operation.

/RD. Read (input, active Low). This signal indicates a read operation and when the Z85X30 is selected, enables the Z85X30's bus drivers. During the Interrupt Acknowledge cycle, /RD gates the interrupt vector onto the bus if the Z85X30 is the highest priority device requesting an interrupt.

/WR. Write (input, active Low). When the Z85X30 is selected, this signal indicates a write operation. This indicates that the CPU wants to write command bytes or data to the Z85X30 write registers.

A//B. Channel A/Channel B (input). This signal selects the channel in which the read or write operation occurs. High selects channel A and Low selects channel B.

D//C. Data/Control Select (input). This signal defines the type of information transferred to or from the Z85X30. High means data is being transferred and Low indicates a command.

1.4.3 Pin Descriptions, (Z80X30 Only)

AD7-AD0. Address/Data Bus (bidirectional, active High, tri-state). These multiplexed lines carry register addresses to the Z80X30 as well as data or control information to and from the Z80X30.

R//W. Read//Write (input, read active High). This signal specifies whether the operation to be performed is a read or a write.

/CS0. Chip Select 0 (input, active Low). This signal is latched concurrently with the addresses on AD7-AD0 and must be active for the intended bus transaction to occur.

CS1. Chip Select 1 (input, active High). This second select signal must also be active before the intended bus transaction can occur. CS1 must remain active throughout the transaction.

/DS. Data Strobe (input, active Low). This signal provides timing for the transfer of data into and out of the Z80X30. If /AS and /DS are both Low, this is interpreted as a reset.

/AS. Address Strobe (input, active Low). Address on AD7-AD0 are latched by the rising edge of this signal.