CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The Z16C35, ISCC™ is a CMOS superintegration device with a flexible Bus Interface Unit (BIU) connecting a built-in Direct Memory Access (DMA) cell to the CMOS Serial Communications Control (SCC) cell.

The ISCC is a dual-channel, multi-protocol data communications peripheral which easily interfaces to CPU's with either multiplexed or non-multiplexed address and data buses. The advanced CMOS process offers lower power consumption, higher performance, and superior noise immunity. The programming flexibility of the internal registers allow the ISCC to be configured for a wide variety of serial communications applications. The many on-chip features such as streamlined bus interface, four channel DMA, baud rate generators, digital phase-locked loops, and crystal oscillators dramatically reduce the need for external logic. Additional features, including a 10x19 bit status FIFO, are added to support high speed SDLC transfers using on-chip DMA controllers.

The ISCC can address up to 4 gigabytes per DMA channel by using the /UAS and /AS signals to strobe out 32-bit multiplexed addresses.

The ISCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (terminals, printers, diskette, tape drives, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ISCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The standard Zilog interrupt daisy chain is supported for interrupt hierarchy control. Internally, the SCC cell has higher interrupt priority than the DMA cell.

The DMA cell consists of four DMA channels; one for transmit and one for receive to and from each SCC channel, respectively.

The DMA cell adopts a simple fly-by-mode DMA transfer, providing a powerful and efficient DMA access. The cell does not support memory-to-memory transfer.

Priorities between the four DMA channels are programmable to custom-fit user applications. Arbitration of Bus priority control signals between the ISCC DMA and other system DMA's should be handled outside the ISCC.

The BIU has a universal interface to most system/CPU bus structures and timing. The first write to the ISCC after a hardware reset will configure the bus interface type being implemented.

1.1 INTRODUCTION (Continued)

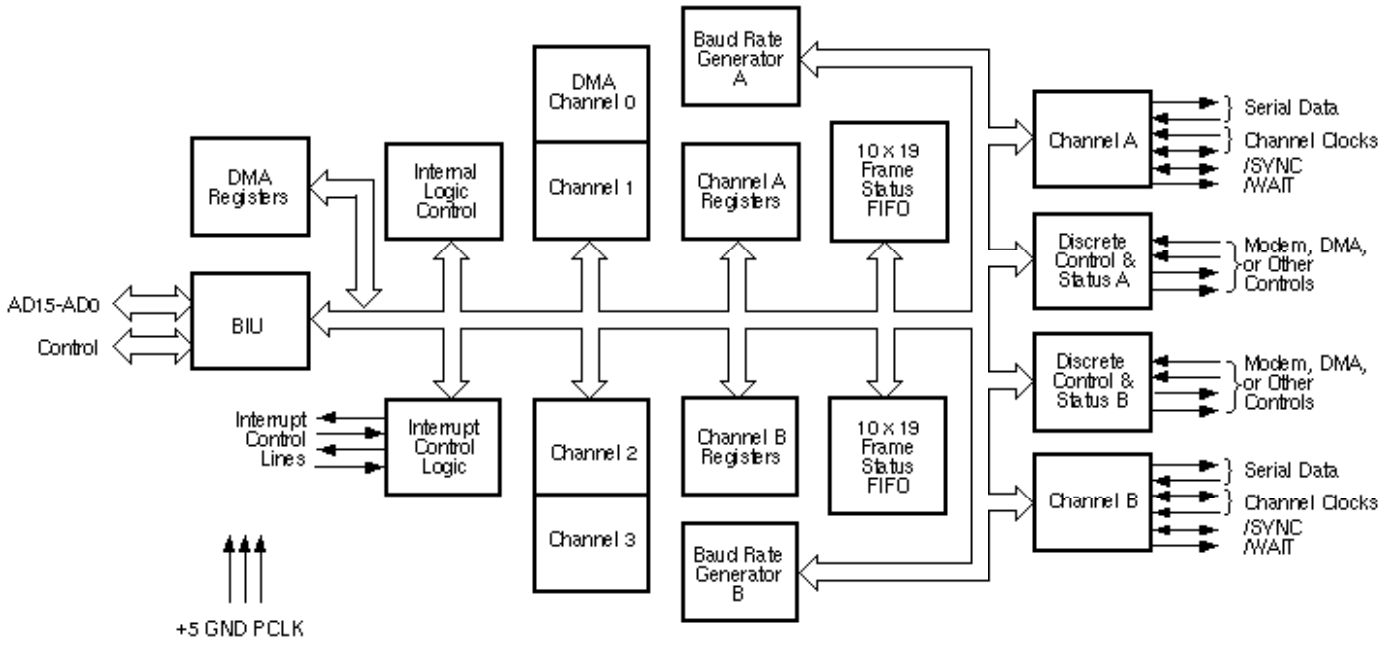

Figure 1-1. Block Diagram

1.2 FEATURES

- Low Power CMOS Technology
- Two General-Purpose SCC Channels, Four DMA Channels; and Universal Bus Interface Unit
- Software Compatible to the Zilog CMOS SCC
- Four DMA Channels; Two Transmit and Two Receive Channels to and from the SCC
- Four Gigabyte Address Range per DMA Channel
- Flyby DMA Transfer Mode
- Programmable DMA Channel Priorities
- Independent DMA Register Set
- A Universal Bus Interface Unit Providing Simple Interface to Most CPUs Multiplexed or Non-Multiplexed Bus; Compatible with 680X0 and 8X86 CPUs
- 32-Bit Addresses Multiplexed to 16-pin Address/Data Lines
- 8-Bit Data Supporting High/Low Byte Swapping
- 10 MHz Timing
- 12.5 and 16 MHz Timing Planned
- 68-Pin PLCC
- Supports all Zilog CMOS SCC Features:
- Two Independent, 0 to 4.0 Mbit/Second, Full-Duplex Channels, Each with a Separate Crystal Oscillator, Baud Rate Generator, and Digital Phase-Locked Loop Circuit for Clock Recovery.
- Multi-Protocol Operation under Program Control; Programmable for NRZ, NRZI, or FM Data Encoding.
- Asynchronous Mode with Five to Eight Bits and One, One and One-Half, or Two Stop Bits per Character; Programmable Clock Factor; Break Detection and Generation; Parity, Overrun, and Framing Error Detection.
- Synchronous Mode with Internal or External Character Synchronization on One or Two Synchronous Characters and CRC Generation and Checking with CRC-16 or CRC-CCITT preset to either 1's or 0's.
- SDLC/HDLC Mode with Comprehensive Frame-Level Control, Automatic Zero Insertion and Deletion, I-Field Residue Handling, Abort Generation and Detection, CRC Generation and Checking, and SDLC Loop Mode Operation.
- Local Loopback and Auto Echo modes
- Supports T1 Digital Trunk
- Enhanced SDLC 10x19 Status FIFO for DMA Support
- Full CMOS SCC Register Set

1.2 FEATURES (Continued)

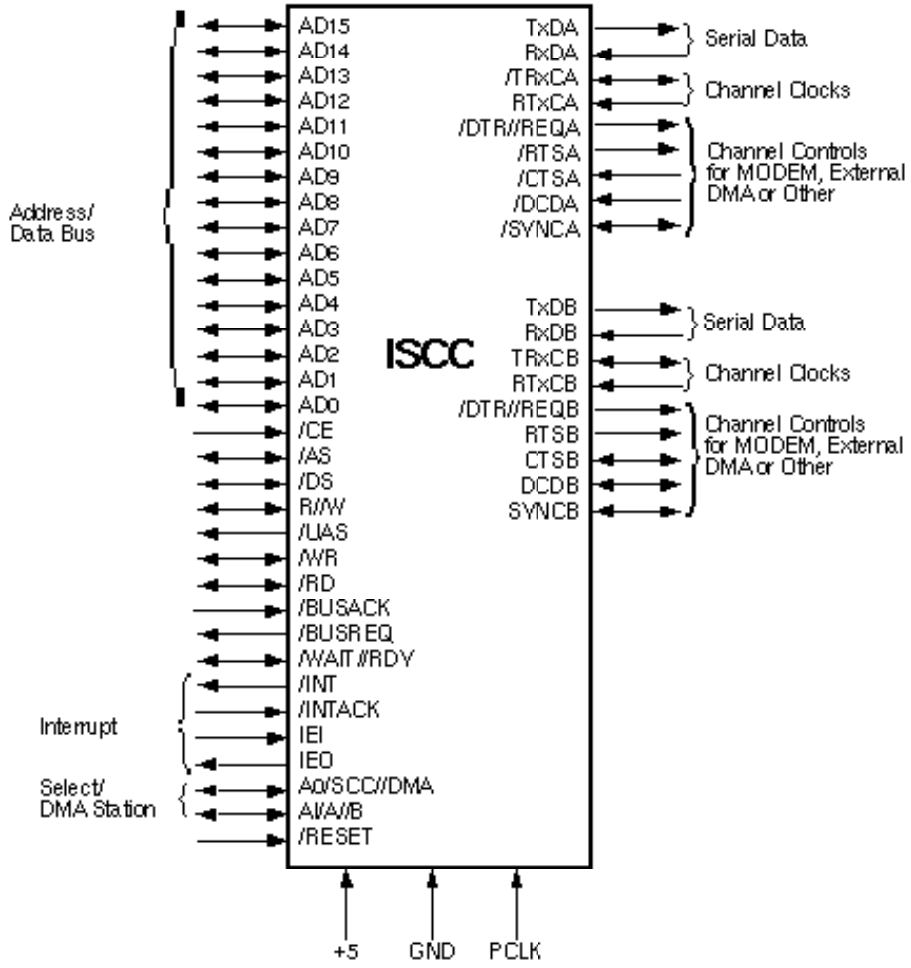

Figure 1-2. Pin Functions

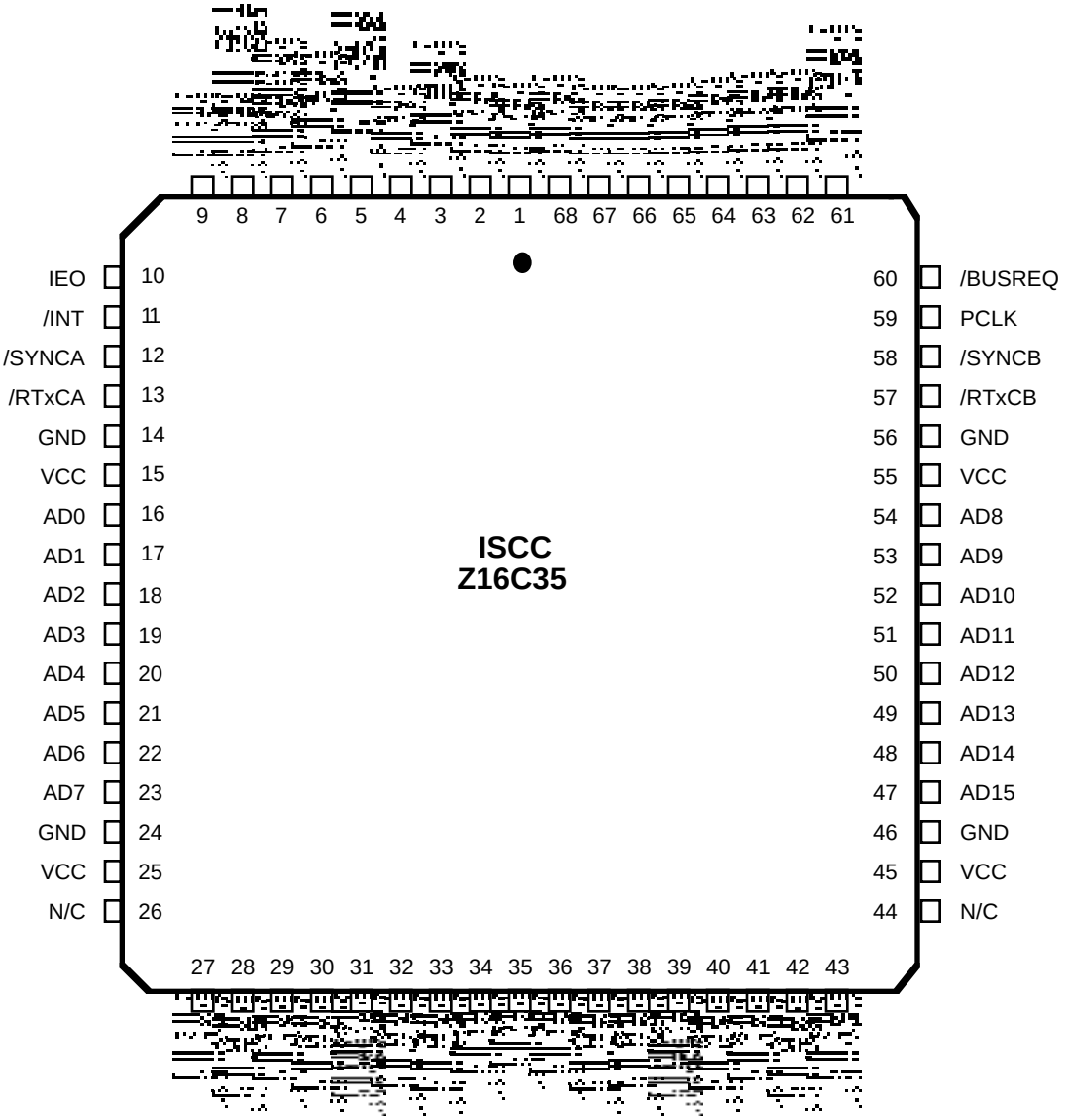

Figure 1-3. Pin Assignments

1.3 PIN DESCRIPTION

The following section describes the Z16C35 pin functions. Figures 1-2 and 1-3 detail the respective pin functions and pin assignments. All references to DMA are internal.

/CTSA, /CTSB. *Clear To Send* (inputs, active Low). These pins function as transmitter enables if they are programmed for Auto Enables (WR3, D5). If these pins are programmed as Auto Enables, a Low on the inputs enables the respective transmitters. If not programmed as Auto Enables, they may be used as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow rise-time inputs. The SCC cell detects transitions on these inputs and can interrupt the CPU on both low to high and high to low transitions.

/DCDA, /DCDB. *Data Carrier Detect* (inputs, active Low). These pins function as receiver enables if they are programmed for Auto Enables (WR3 D5), otherwise they are used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow rise time signals. The SCC cell detects transitions on these inputs and can interrupt the CPU on both low to high and high to low transitions.

/DTR//REQA, /DTR//REQB. *Data Terminal Ready/Request* (outputs, active Low). These pins are programmable (WR14, D2) to serve as either general-purpose outputs or as DMA request lines. When programmed for the DTR function These outputs follow the state programmed into the DTR bit of Write Register 5 (WR5, D7). When programmed for the Ready mode, these pins serve as DMA requests for the transmitter. Note that this DMA request is not associated with the on-chip DMA and is intended for use in requesting DMA service from an external DMA.

IEI. *Interrupt Enable In* (input, active High). IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt driven device. A high IEI indicates that no other higher priority device has an interrupt under service or is requesting an interrupt.

IEO. *Interrupt Enable Out* (output, active High). IEO is High only if IEI is High and the CPU is not servicing the ISCC (SCC or DMA) interrupt or the ISCC is not requesting an interrupt (Interrupt Acknowledge cycle only). IEO is connected to the next lower priority device's IEI input and thus inhibits interrupts from lower priority devices.

/INT. *Interrupt* (output, active Low). This signal is activated when the SCC or DMA requests an interrupt. Note that /INT is pulled high and is not an open-drain output.

/INTACK. *Interrupt Acknowledge* (input, active Low). This is a strobe which indicates that an interrupt acknowledge cycle is in progress. During this cycle, the SCC and DMA interrupt daisy chain is resolved. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle when /RD or /DS become high. /INTACK may be programmed to accept a status acknowledge, a single pulse acknowledge, or a double pulse acknowledge. This is programmed in the Bus Configuration Register (BCR). The double pulse acknowledge is compatible with 8X86 family microprocessors.

PCLK. *Clock* (input). This is the master SCC cell and DMA cell clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.

RxDA, RxDB. *Receive Data* (inputs, active High). These input signals receive serial data at standard TTL levels.

/RTxCA, /RTxCB. *Receive/Transmit Clocks* (inputs, active Low). These pins can be programmed to several modes of operation. In each channel, /RTxC may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the Digital Phase-Locked Loop. These pins can also be programmed for use with the respective /SYNC pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous modes.

/RTSA, /RTSB. *Request To Send* (outputs, active Low). When the Request To Send (RTS) bit in Write Register 5 is set, the /RTS signal goes Low. When the RTS bit is reset in the Asynchronous mode and Auto Enable is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with Auto Enable off, the /RTS pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.

/SYNCA, /SYNCB. *Synchronization* (inputs or outputs, active Low). These pins can act either as inputs, outputs, or part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to /CTS and /DCD. In this mode, transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0 but have no other function.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode, /SYNC must be driven Low two receive clock cycles after the last bit in the synchronous character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.

In the Internal Synchronization mode (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync condition is not latched. These outputs are active each time a sync pattern is recognized

(regardless of character boundaries). In SDLC mode, the pins act as outputs and are valid on receipt of a flag. The output is active for one receive clock period (refer to Chapter 4).

TxDA, TxDB. *Transmit Data* (outputs, active high). These output signals transmit serial data at standard TTL levels.

/TRxCA, /TRxCB. *Transmit/Receive Clocks* (inputs or outputs, active Low). These pins can be programmed in several different modes of operation. /TRxC may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/CE. *Chip Enable* (input, active Low). This signal selects the ISCC for a peripheral read or write operation. This signal is ignored when the ISCC is bus master.

AD15-AD0. *Data bus* (bidirectional, tri-state). These lines carry data and commands to and from the ISCC.

/RD. *Read* (bidirectional, active Low). When the ISCC is a peripheral (i.e., bus slave), this signal indicates a read operation and when the ISCC is selected, enables the ISCC's bus drivers. As an input, /RD indicates that the CPU wants to read from the ISCC read registers. During the Interrupt Acknowledge cycle, /RD gates the interrupt vector onto the bus if the ISCC is the highest priority device requesting an interrupt. When the ISCC is the bus master, this signal is used to read data. As an output, after the ISCC has taken control of the system buses, /RD indicates a DMA-controlled read from a memory or I/O port address.

/WR. *Write* (bidirectional, active Low). When the ISCC is selected, this signal indicates a write operation. As an input, this indicates that the CPU wants to write control or command bytes to the ISCC write registers. As an output, after the ISCC has taken control of the system buses /WR indicates a DMA-controlled write to a memory or I/O port address.

/DS. *Data Strobe* (bidirectional, active Low). A Low on this signal indicates that the AD15-AD0 bus is used for data transfer. When the ISCC is not in control of the system bus and the external system is transferring information to or from the ISCC, /DS is a timing input used by the ISCC to move data to or from the AD15-AD0 bus. Data is written into the ISCC by the external system on the High to Low /DS transition. Data is read from the ISCC by the external system while /DS is Low. There are no timing requirements between /DS as an input and ISCC clock; this allows use of the ISCC with a system bus which does not have a bussed clock.

During a DMA operation when the ISCC is in control of the system, /DS is an output generated by the ISCC and used by the system to move data to or from the AD15-AD0 bus. When the ISCC has bus control, it writes to the external system by placing data on the AD15-AD0 bus before the High-to-Low /DS transition and holds the data stable until after the Low-to-High /DS transition; while reading from the external system, the Low-to-High transition of /DS inputs data from the AD15-AD0 bus into the ISCC.

R//W. *Read/Write* (bidirectional). Read polarity is High and write polarity is Low. When the ISCC is not in control of the system bus and the external system is transferring information to or from the ISCC, R//W is a status input used by the ISCC to determine if data is entering or leaving on the AD15-AD0 bus during /DS time. In such a case, Read (High) indicates that the system is requesting data from the ISCC and Write (Low) indicates that the system is presenting data to the ISCC. The only timing requirements for R//W as an input are defined relative to /DS. When the ISCC is in control of the system bus, R//W is an output generated by the ISCC, with Read (high) indicating that data is being requested from the addressed location or device, and Write (low) indicating that data is being presented to the addressed location or device.

/UAS. *Upper Address Strobe* (Output, active Low). This signal is used if the output address is more than 16-bit. The upper address, A31-A16, can be latched externally by the rising edge of this signal. /UAS is active first before /AS becomes active. This signal and /AS are used by the DMA cell.

/AS. *Lower Address Strobe* (bidirectional, active Low). When the ISCC is bus master, this signal is an output, and is used as a lower address strobe for AD15-AD0. It is used in conjunction with /UAS since the address is 32-bits. This signal and /UAS are used by the DMA cell when it is bus master. When ISCC is not bus master, this signal is used in the multiplexed bus modes to latch the address on the AD lines. The /AS signal is not used in the non-multiplexed bus modes and should be tied to V_{CC} through a resistor in these cases.

/WAIT//RDY. *Wait/Ready* (bidirectional, active Low). This signal may be programmed to function either as a Wait signal or Ready signal during the BCR write. When the BCR is written to Channel A (A1/A//B High during the BCR write), this signal functions as a /WAIT and thus supports the READY function of 8X86 microprocessors family. When the BCR writes to Channel B (A1/A//B Low), this signal functions as a /READY and supports the /DTACK function of the 680X0 microprocessor family.

This signal is an output when the ISCC in not bus master. In this case, the /Wait//RDY signal indicates when the data is available during a read cycle; when the device is ready to receive data during a write cycle; and when a valid vector is available during an interrupt acknowledge cycle.

1.3 PIN DESCRIPTION (Continued)

When the ISCC is the bus master (the DMA cell has taken control of the bus), the /Wait//RDY signal functions as a /WAIT or /READY input. Slow memories and peripheral devices can assert /WAIT to extend /DS during bus transfers. Similarly, memories and peripherals use /READY to indicate that its output is valid or that it is ready to latch input data.

/BUSACK. *Bus Acknowledge* (input, active Low). Signals the bus has been released to the DMA. If the /BUSACK goes inactive before the DMA transfer is completed, the current DMA transfer is aborted.

/BUSREQ. *Bus Request* (output, active Low). This signal is used by the DMA to obtain the bus from the CPU.

A0/SCC//DMA. *DMA Channel/SCC Select/DMA Select* (bidirectional). When this pin is used as input, a high selects the SCC cell and a low selects the DMA cell, (during BCR Write should be kept Low). When this pin is used as output, the signal on this pin is used in conjunction with A1/A//B pin output to identify which DMA channel is active. This information can be used by the user to determine whether to issue a DMA abort command. A0/SCC//DMA and A1/A//B output encoding is shown on the following page.

A1/A//B	A0/SCC//DMA	DMA channel
1	1	RxA
1	0	TxA
0	1	RxB
0	0	TxB

A1/A//B. *DMA Channel/Channel A/Channel B* (bidirectional). This signal, when used as input, selects the SCC channel in which the read and write operation occurs. Note that A0/SCC//DMA pin must be held high to select this feature. When this pin is used as an output, it is used in conjunction with the A0/SCC//DMA pin output to identify which DMA channel is active. During a DMA peripheral access, the A1/A//B pin is ignored.

/RESET. (input, active Low). This signal resets the device to a known state. The first write to the ISCC after a reset accesses the BCR to select additional bus options for the device.